Designation: F 1529 – 02

Standard Test Method for Sheet Resistance Uniformity Evaluation by In-Line Four-Point Probe with the Dual-Configuration Procedure[1]

This standard is issued under the fixed designation F 1529; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

INTRODUCTION

This test method uses a four-point probe in a manner different from that of other ASTM methods for the measurement of the resistivity or sheet resistance of semiconductors. In this test method, two different ways (configurations) of connecting the probe pins to the electronics that supply current and measure voltage are used at each measurement location on the specimen. This use of a four-point probe is often referred to as "dual-configuration" or as "configuration switched" measurements.

There are three benefits that result from the second measurement configuration at each location: (*1*) the probe no longer needs to be in a high symmetry orientation on the specimen, that is, being perpendicular or parallel to the radius on a circular wafer or to the length or width of a rectangular specimen, as long as it is a modest distance from the edge of the wafer, (*2*) the lateral dimension(s) of the specimen, and the exact location of the probe on the specimen no longer have to be known—the geometric scaling factor results directly f rom the two sets of electrical measurements at each location, (*3*) the two sets of measurements self-correct for the actual separations between the probe pins in a manner that has been shown to be more effective than measuring probe impressions made on a piece of polished material. As a result, high precision measurements can be made with smaller probe separations than is possible with single configuration use of a four-point probe, thus allowing higher spatial resolution of wafer sheet resistance variations. **(1)**[2]

1. Scope

1.1 This test method covers the direct measurement of the sheet resistance and its variation for all but the periphery (amounting to three probe separations) for circular conducting layers pertinent to silicon semiconductor technology. These layers may be fabricated on substrates of any diameter that is capable of being securely mounted on a prober stage.

NOTE 1—The equation used to calculate the sheet resistance data from measurements is not perfectly accurate out to the edge of the wafer for probes oriented at an arbitrary angle with respect to a wafer radius. Further, automatic instruments on which this test method will be performed may not have perfect centering of the wafer on the measurement stage. These factors require that the periphery of the layer being measured be excluded. Also, many thin film processes use wafer clamps that preclude forming layers out to the edge of the substrate. The edge exclusion in this test method applies to the film that is being measured, rather than to the substrate. The equation used is based on mathematics developed for layers of circular shape. It is expected to work well for layers of other shapes such as rectangular, if edge exclusion requirements are met; however, the accuracy near the edge of other shapes has not been demonstrated **(2).**

1.2 This test method is intended primarily for assessing the uniformity of layers formed by diffusion, epitaxy, ion implant and chemical vapor, or other deposition processes on a silicon substrate. The deposited film, which may be single crystal, polycrystalline or amorphous silicon, or a metal film, must be electrically isolated from the substrate. This can be accomplished if the layer is of opposite conductivity type from the substrate or is deposited over a dielectric layer such as silicon dioxide. This test method is capable of measuring films as thin as 0.05 µm, but particular care is required for establishing reliable measurements for most films in the range below 0.2 µm. Films that have a thickness up to half the probe separation can be measured without the use of a thickness-related correction factor. It may give misleading results for films formed by silicon on insulator technologies because of charge or charge trapping in the insulator.

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved Dec. 10, 2002. Published February 2003. Originally approved in 1994. Last previous edition approved in 1997 as F 1529 – 97.

[2] The boldface numbers in parentheses refer to the list of references at the end of this test method.

1.3 This test method can be used to measure the sheet resistance uniformity of bulk substrates. However, the thickness of the substrate must be known to be constant or must be measured at all positions where sheet resistance values are measured in order to calculate relative variations in resistance reliably.

NOTE 2—The thickness correction factor for layers that are thicker than 0.5 times the probe spacing is known to vary more rapidly than that for single-configuration four-probe measurements, but such a correction has not yet been published. Until such a correction is published, resistivity values determined by the dual-configuration method will not be accurate for these thicker specimens; however, if the wafer has uniform thickness, variations of resistivity can still be determined by this test method.

1.4 This test method can be used to measure sheet resistance values from below 10 mΩ for metal films, to over 25 000 Ω for thin silicon films. However, for films at the upper end of this resistance range, and for films toward the low end of the thickness range, the interpretation of the sheet resistance values may not be straightforward due to various semiconductor effects **(3, 4, 5)**.

NOTE 3—The principles of this test method are also applicable to other semiconductor materials, but the appropriate conditions and the expected precision have not been established.

1.5 This test method uses two different electrical configurations of the four-point probe at each measurement location. It does not require measurement of probe location on the wafer, or probe separations, or of wafer diameter (except to determine edge exclusion for measurement-site selection) as do other four-point probe methods such as Test Methods F 81, F 84 and F 374. By use of electrical data from the two different configurations at each location, the method is self-calibrating with respect to the geometrical parameters **(1)**.

1.6 This test method is intended to be used on automated wafer testing systems that use *R*-theta or *X*-*Y* stage positioning for the measurements. The rapid calculations for sheet resistance used in this test method are based on more extensive calculations, and are within 0.1 % of the results of those more extensive calculations, even if the probes are not oriented parallel or perpendicular to a wafer radius, providing that the probes are more than 3-probe spacings from the edge of the layer being measured **(1)**, **(2)** (see Note 1).

1.7 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

D 5127 Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industry[3]

F 42 Test Methods for Conductivity Type of Extrinsic Semiconducting Materials[4]

F 81 Test Method for Measuring Radial Resistivity Variation on Silicon Slices[4]

F 84 Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe[4]

F 374 Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-Implanted Layers Using an In-Line Four-Point Probe[4]

F 1241 Terminology of Silicon Technology[4]

2.2 *SEMI Standards:*

SEMI C19 Specification for Acetone[5]

SEMI C23 Specifications for Buffered Oxide Etchants[5]

SEMI C41 Specifications and Guidelines for 2-Propanol[5]

3. Terminology

3.1 *Definitions:*

3.1.1 For definitions of terms used in silicon wafer technology refer to Terminology F 1241.

4. Summary of Test Method

4.1 An in-line four-point probe is used to determine the specimen sheet resistance at each desired measurement location. The number and positioning of measurement locations is determined by end-use needs, or by the parties to the test in the case of referee measurements. At each location, a direct current is passed into the specimen, using two of the probes, as specified, and the potential difference is measured using the other two probes. Current polarity is reversed and the potential difference is remeasured to allow elimination of thermoelectric effects. Before the probe is raised, the process is repeated using a different combination of probes, as specified. At each location, the sheet resistance is obtained from the four ratios of potential difference to current.

4.2 The adequacy of the probe is determined both by optical examination of probe indentations made in a polished silicon surface, and by a performance test on a wafer of the type whose uniformity is to be checked.

4.3 The accuracy of the electronics is tested by means of an analog circuit emphasizing the performance and noise immunity of the electronics in the presence of large contact resistances of the probe tips to the semiconductor surface.

5. Significance and Use

5.1 The sheet resistance of epitaxial, implanted, diffused or deposited films is an important materials acceptance and process control parameter. The uniformity across a wafer of the sheet resistance resulting from any of these processes is important for the equivalence of performance of devices or circuits made from various regions of the wafer.

5.2 This test method is suitable for use in materials acceptance, equipment qualification, process control, research, and development.

[3] *Annual Book of ASTM Standards*, Vol 11.01.

[4] *Annual Book of ASTM Standards*, Vol 10.05.

[5] Available from Semiconductor Equipment and Materials International, 3081 Zanker Road, San Jose, CA 95134 (www.semi.org).

6. Interferences

6.1 Photoconductive and photovoltaic effects can seriously influence the measured sheet resistance, particularly with high resistivity layers or those with very shallow junctions. Therefore, all measurements should be made in a darkened enclosure unless experience shows that the material of interest is insensitive to ambient illumination.

6.2 Spurious currents can be induced in the test circuit when the equipment is located near high-frequency generators. If such a location is unavoidable, adequate shielding must be provided.

6.3 Minority carrier injection during the measurement can occur due to the electric field in the specimen. With material possessing a long minority-carrier lifetime and moderate to high resistivity, such injection can result in a lowering of the resistivity (sheet resistance) for a distance of several centimetres from the point of injection. Carrier injection can be detected by repeating the measurements at lower current. In the absence of injection, no increase in resistivity should be observed at the lower current. The current level recommended, (see Table 1) should reduce the probability of difficulty from this interference to a minimum, but in cases of doubt the measurements should be repeated at a lower current level. If the proper current is being used, doubling or halving its value should result in a change of sheet resistance that is less than 0.5 %.

6.4 Semiconductors have a significant temperature coefficient of resistivity. Consequently, the measurement current used should be small to avoid resistive heating. The current levels recommended should reduce the chances of this problem. If resistive heating is suspected, it can be detected by a change in readings starting immediately after the current is applied. If such a change is observed, repeat the electrical measurements at a lower current. In the absence of Joule heating, the temperature of the water should be uniform if the wafer is mounted on a chuck having good thermal conductivity and large thermal mass. Sheet resistance maps should not be distorted by temperature nonuniformities in this case. Coefficients for the temperature variation of the sheet resistance of a particular layer type will depend upon the specific dopant, or resistivity, profile of that layer type, and must be evaluated empirically for the layer fabrication process being used if correction of data to a fixed reference temperature is desired.

6.5 Vibration of the probe may cause variations in contact resistance, which is often manifested as unstable readings. If difficulty is encountered, the apparatus should be vibration isolated.

TABLE 1 Nominal Current Values for Measurement of Sheet Resistance

Sheet Resistance, Ω	Current [A]
2–25	10 mA
20–250	1 mA
200–2500	100 µA
2000–25 000	10 µA

[A] The current used should be from one-half to twice the nominal value and should be chosen to give a measured voltage on the specimen that is between 7 and 15 mV when using Configuration A. Once the current is selected for forward direction measurements at a given site, it must be kept constant to 0.01 % for the remaining measurements at that site.

6.6 Penetration of either the current or voltage probes through the layer being measured to the substrate will result in erroneous readings. This can usually be checked by mounting the specimen directly on a metal support that is grounded to the current supply and by then looking for a reduction in measured specimen voltage in at least one polarity as the ground connection is removed and replaced. If this condition occurs, examine the probe tips microscopically for sharp asperities and remove these by polishing or otherwise conditioning the probe tip, or else reduce the probe force or use a probe with blunter probe tips.

6.7 Use of two electrical configurations at each measurement site eliminates the need for measurement of geometric separation of the probe tips in order to analyze the data. As a result, even for referee measurements, any probe spacing that is agreed upon between the parties to the test and demonstrates sufficiently low data scatter may be used for this test method.

6.8 Use of the data from the two electrical configurations to calculate a factor for water diameter and for position of the measurement site on the wafer will be accurate to within 0.1 % as long as the measurement site is away from the perimeter of the wafer. To meet this requirement the site should be at least five-probe separations from the perimeter for the case of probe alignment perpendicular to a wafer diameter, and at least three-probe separations from the perimeter for the case of probe alignment parallel to a wafer diameter. For certain processes, such as ion implantation, use of a wafer clamp during layer formation causes a p-n layer-to-substrate junction on the top surface of the wafer interior to the mechanical edge of the wafer. In these cases, the probe separation values above refer to the location of the measurement site with respect to such junctions.

6.9 In shallow or lightly-doped layers, an effect known as carrier redistribution will cause the number of free carriers in the layer to be different from the number of dopant atoms. As a result, sheet resistance values measured by this test method may be noticeably different from values calculated from models that imply the dopant and free-carrier depth profiles to be equivalent.

6.10 Surface and near-surface effects, such as the formation of hydrogen complexes with acceptors, may occur during or immediately after the fabrication of many thin films, particularly if lightly doped. They may also occur slowly with storage. These effects may be uniformly or nonuniformly distributed across the wafer surface. The result is to modify, generally by way of increasing, the measured sheet resistance. Two of the most prominent impacts of these effects are to make the results of a given process step appear to be more nonuniform than is actually the case, and to shift the absolute level of a reference wafer used to monitor the performance of the mapping tool so as to make the tool appear to be out of control.

7. Apparatus

7.1 *Specimen Preparation*:

7.1.1 *Chemical Laboratory Apparatus*, such as plastic beakers, graduated cylinders, and plastic coated tweezers for use both with acids and with solvents. Proper facilities for handling and disposing of acids and their vapors are essential.